FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11216-1E

MEMORY

CMOS

1 M × 32 BITS FAST PAGE MODE DRAM MODULE

MB85341C-60/-70

CMOS 1,048,576 × 32 BITS Fast Page Mode DRAM Module

■ DESCRIPTION

The Fujitsu MB85341C is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB814400C devices. The MB85341C is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85341C are the same as the MB814400C which features fast page mode operation. For ease of memory expansion, the MB85341C is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB85341C-60	MB85341C-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		110 ns min.	125 ns min.
Address Access Time		30 ns max.	35 ns max.
$\overline{CAS}$ Access Time		15 ns max.	20 ns max.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Power Dissipation	Operating Mode	2684 mW max.	2376 mW max.
	Standby Mode	88 mW max.	88 mW max.
	Self Refresh Mode	44 mW max.	44 mW max.

- Organization: 1,048,576 words × 32 bits
- Memory: MB814400C, 8 pcs
- Decoupling Capacitor: 16 pcs
- 5.0 V±10% Supply Voltage
- 1,024 Refresh Cycles / 16.4 ms
- Fast page mode operation
- Package and Ordering Information:
  72-pad SIMM, order as
  MB85341C-××PJPBK
  (PJPBK = Gold Pad)
  MB85341C-××PJPB
  (PJPB = Solder Pad)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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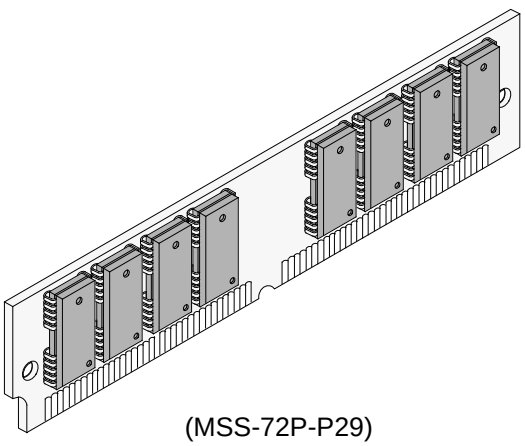
■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8	W
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

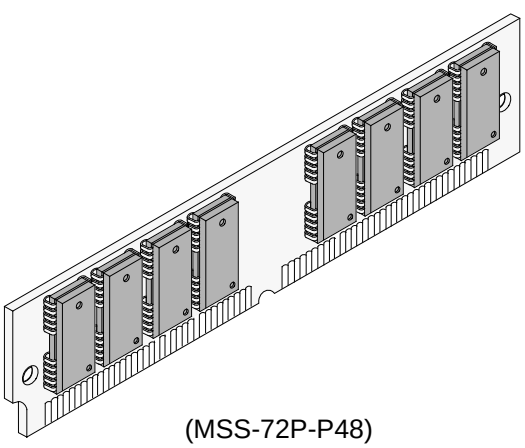
■ PACKAGE

72-pin plastic SIMM (socket type)



(MSS-72P-P29)

72-pin plastic SIMM (socket type)

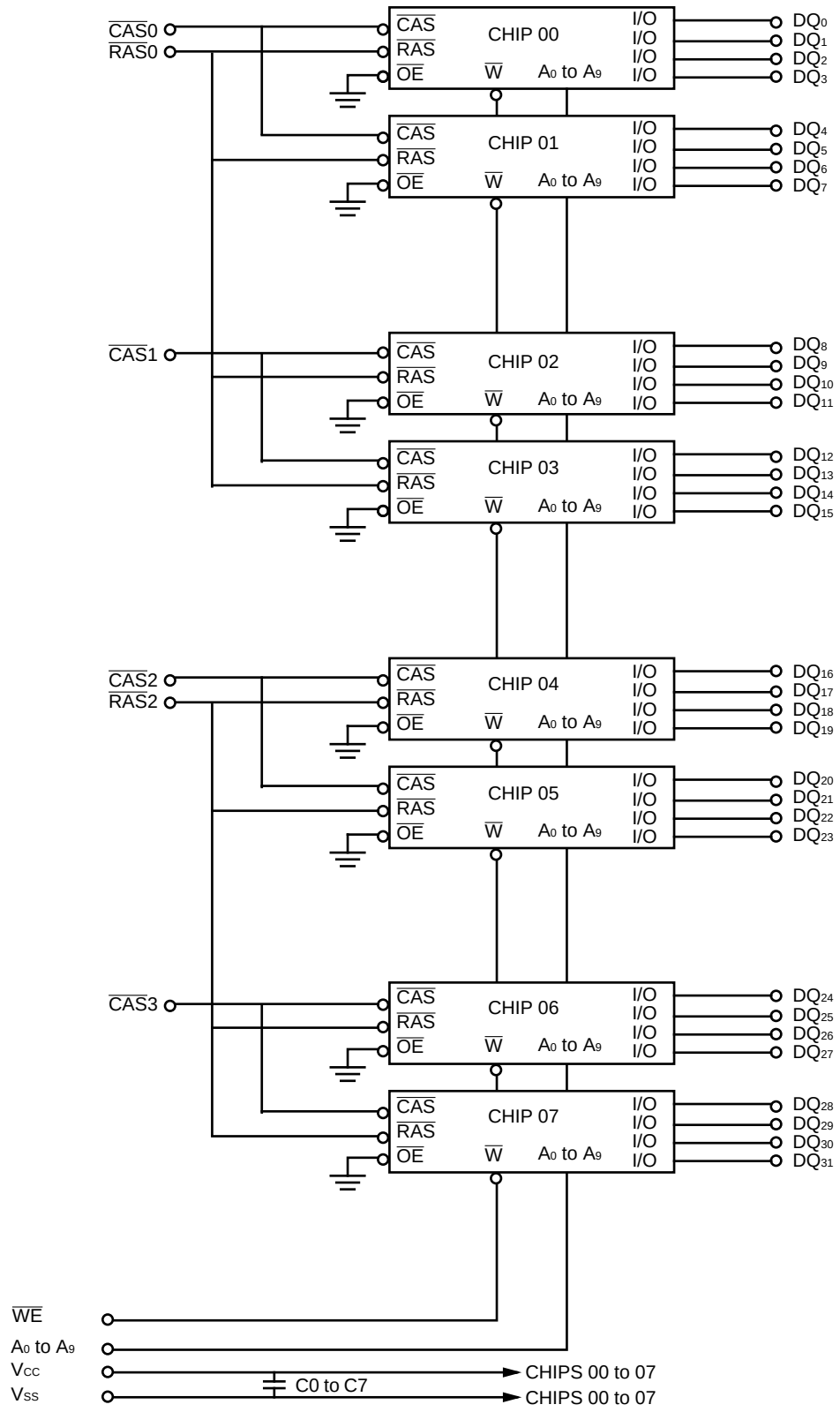


(MSS-72P-P48)

DQ_0	2	1	V_{SS}
DQ_1	4	3	DQ_{16}
DQ_2	6	5	DQ_{17}
DQ_3	8	7	DQ_{18}
V_{CC}	10	9	DQ_{19}
A_0	12	11	N.C.
A_2	14	13	A_1
A_4	16	15	A_3
A_6	18	17	A_5
DQ_4	20	19	N.C.
DQ_5	22	21	DQ_{20}
DQ_6	24	23	DQ_{21}
DQ_7	26	25	DQ_{22}
A_7	28	27	DQ_{23}
V_{CC}	30	29	N.C.
A_9	32	31	A_8
$\overline{RAS2}$	34	33	N.C.
N.C.	36	35	N.C.
N.C.	38	37	N.C.
$\overline{CAS0}$	40	39	V_{SS}
$\overline{CAS3}$	42	41	$\overline{CAS2}$
$\overline{RAS0}$	44	43	$\overline{CAS1}$
N.C.	46	45	N.C.
N.C.	48	47	$\overline{WE}$
DQ_{24}	50	49	DQ_8
DQ_{25}	52	51	DQ_9
DQ_{26}	54	53	DQ_{10}
DQ_{27}	56	55	DQ_{11}
DQ_{28}	58	57	DQ_{12}
DQ_{29}	60	59	V_{CC}
DQ_{30}	62	61	DQ_{13}
DQ_{31}	64	63	DQ_{14}
N.C.	66	65	DQ_{15}
PD_2	68	67	PD_1
PD_4	70	69	PD_3
V_{SS}	72	71	N.C.

Pin #	Symbol	-60	-70
67	PD_1	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}
69	PD_3	N.C.	V_{SS}
70	PD_4	N.C.	N.C.

FUNCTIONAL BLOCK DIAGRAM



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■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, All Inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –5.0 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = +4.2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V; 4.5 V ≤ V_{CC} ≤ 5.5 V; V_{SS} = 0 V, All other pins not under test = 0 V	–30	30	µA
		$\overline{CAS}$			–20	20	
		Address, $\overline{WE}$			–60	60	
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V; Data out disabled	–10	10	µA
Operating Current (Average Power Supply Current)	*2	MB85341C-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	488	mA
		MB85341C-70			—	432	
Standby Current (Power Supply Current)		TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	16	mA
		CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	8	
Refresh Current #1 (Average Power Supply Current)	*2	MB85341C-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling; t_{RC} = min	—	488	mA
		MB85341C-70			—	432	
Fast Page Mode Current	*2	MB85341C-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min	—	328	mA
		MB85341C-70			—	296	
Refresh Current #2 (Average Power Supply Current)	*2	MB85341C-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	392	mA
		MB85341C-70			—	352	
Refresh Current #3 (Average Power Supply Current)		MB85341C-60	I_{CC9}	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2 V, Self Refresh	—	8	mA
		MB85341C-70			—	8	

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	—	61	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}	—	34	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}	—	23	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	55	pF
Input/Output Capacitance, DQ_0 to DQ_{31}	C_{DQ}	—	11	pF

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB85341C-60		MB85341C-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	—	70	ns
4	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	15	—	20	ns
5	Column Address Access Time	*6,7	t_{AA}	—	30	—	35	ns
6	Output Hold Time		t_{OH}	0	—	0	—	ns
7	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	ns
8	Output Buffer Turn off Delay Time	*8	t_{OFF}	—	15	—	15	ns
9	Transition Time		t_T	2	50	2	50	ns
10	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
11	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
12	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	ns
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*9,10	t_{RCD}	20	45	20	50	ns
15	$\overline{CAS}$ Pulse Width		t_{CAS}	15	10000	20	10000	ns
16	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
17	$\overline{CAS}$ Precharge Time (Normal)	*15	t_{CPN}	10	—	10	—	ns
18	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
19	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
20	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
21	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
22	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	15	30	15	35	ns
23	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
24	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0	—	0	—	ns
28	Write Command Set Up Time	*13	t_{WCS}	0	—	0	—	ns
39	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	18	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB85341C-60		MB85341C-70		Unit
				Min.	Max.	Min.	Max.	
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	ns
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	5	—	5	—	ns
36	$\overline{CAS}$ Set Up Time (C-B-R Refresh)		t_{CSR}	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	10	—	10	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$	*17	t_{WSR}	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$	*17	t_{WHR}	10	—	10	—	ns
40	DIN to $\overline{CAS}$ Delay Time		t_{DZC}	0	—	0	—	ns
41	Fast Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	200000	—	200000	ns
42	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
43	Access Time from $\overline{CAS}$ Precharge	*7,14	t_{CPA}	—	35	—	40	ns
44	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
45	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
46	$\overline{RAS}$ Pulse Width for Self Refresh	*16	t_{RASS}	100	—	100	—	µs
47	$\overline{RAS}$ Precharge Time for Self Refresh	*16	t_{RPS}	110	—	125	—	ns
48	$\overline{CAS}$ Hold Time for Self Refresh	*16	t_{CHS}	–50	—	–50	—	ns

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Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles ($\overline{WE}$ = V_{IH}) before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 2 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} and/or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF} is specified that output buffer change to high-impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).

*15. Assumes $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

*16. Assumes $\overline{CAS}$-before-$\overline{RAS}$ Self Refresh cycle.

*17. Assumes test mode function.

*Source: See MB814400C Data Sheet for details on the electricals.

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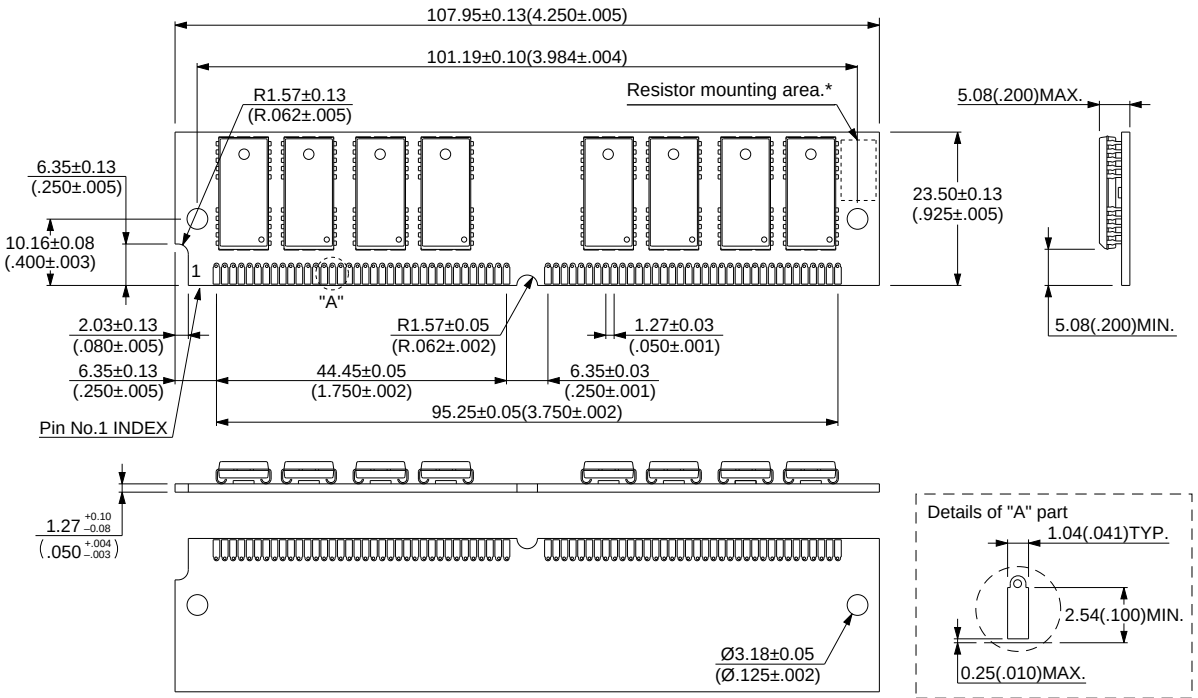
■ PACKAGE DIMENSIONS

(Suffix: PJPBK)

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P29)



* Resistor thickness is 1.00 mm (.0.4 in.) maximum from board surface.

Dimensions in mm (inches)

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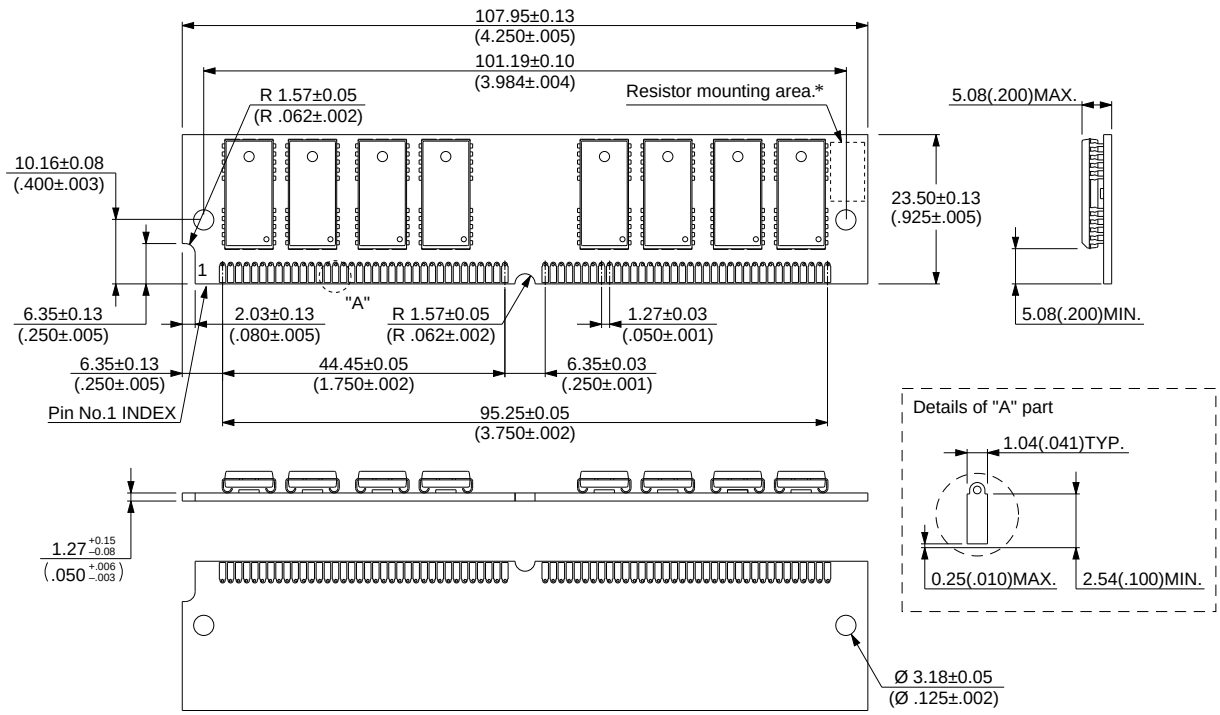
■ PACKAGE DIMENSIONS

(Suffix: PJPBK)

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P48)



* Resistor thickness is 1.00 mm (.0.4 in.) maximum from board surface.

Dimensions in mm (inches)

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